

## CLAIMS

1 1. A CMOS inverter comprising:

2 a heterostructure including a Si substrate, a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer on said Si substrate,

3 and a strained surface layer on said relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer; and

4 a pMOSFET and an nMOSFET, wherein the channel of said pMOSFET and the

5 channel of said nMOSFET are formed in said strained surface layer.

1 2. The CMOS inverter of claim 1, wherein the heterostructure further comprises a

2 planarized surface positioned between the strained surface layer and the Si substrate.

1 3. The CMOS inverter of claim 1, wherein the surface roughness of the strained surface

2 layer is less than 1nm.

1 4. The CMOS inverter of claim 1, wherein the heterostructure further comprises an oxide

2 layer positioned between the relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer and the Si substrate.

1 5. The CMOS inverter of claim 1, wherein the heterostructure further comprises a SiGe

2 graded buffer layer positioned between the relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer and the Si substrate.

1 6. The CMOS inverter of claim 1, wherein the strained surface layer comprises Si.

1 7. The CMOS inverter of claim 1, wherein  $0.1 < x < 0.5$ .

1 8. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the

2 gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the

3 hole mobility in bulk silicon.

1 9. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the  
2 gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the  
3 hole mobility in the strained surface layer.

1 10. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to  
2 the gate width of the nMOSFET is approximately equal to the square root of the ratio of the  
3 electron mobility and the hole mobility in bulk silicon.

1 11. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to  
2 the gate width of the nMOSFET is approximately equal to the square root of the ratio of the  
3 electron mobility and the hole mobility in the strained surface layer.

1 12. The CMOS inverter of claim 7, wherein the gate drive is reduced to lower power  
2 consumption.

1 13. In a high speed integrated circuit, the CMOS inverter of claim 7.

1 14. In a low power integrated circuit, the CMOS inverter of claim 7.

1 15. An integrated circuit comprising:

2 a heterostructure including a Si substrate, a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer on said Si substrate,  
3 and a strained layer on said relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer; and

4 a p transistor and an n transistor formed in said heterostructure, wherein said strained  
5 layer comprises the channel of said n transistor and said p transistor, and said n transistor and

6 said p transistor are interconnected in a CMOS circuit.

1 16. The integrated circuit of claim 15, wherein the heterostructure further comprises a  
2 planarized surface positioned between the strained layer and the Si substrate.

1 17. The integrated circuit of claim 15, wherein the surface roughness of the strained layer  
2 is less than 1nm.

1 18. The integrated circuit of claim 15, wherein the heterostructure further comprises an  
2 oxide layer positioned between the relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer and the Si substrate.

1 19. The integrated circuit of claim 15, wherein the heterostructure further comprises a SiGe  
2 graded buffer layer positioned between the relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer and the Si substrate.

1 20. The integrated circuit of claim 15, wherein the strained layer comprises Si.

1 21. The integrated circuit of claim 15, wherein  $0.1 < x < 0.5$ .

1 22. The integrated circuit of claim 15, wherein the CMOS circuit comprises a logic gate.

1 23. The integrated circuit of claim 15, wherein the CMOS circuit comprises a NOR gate.

1 24. The integrated circuit of claim 15, wherein the CMOS circuit comprises an XOR gate.

1 25. The integrated circuit of claim 15, wherein the CMOS circuit comprises a NAND gate.

1 26. The integrated circuit of claim 15, wherein the p-channel transistor serves as a pull-up  
2 transistor in said CMOS circuit and the n-channel transistor serves as a pull-down transistor in

3 said CMOS circuit.

1 27. The integrated circuit of claim 15, wherein the CMOS circuit comprises an inverter.

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